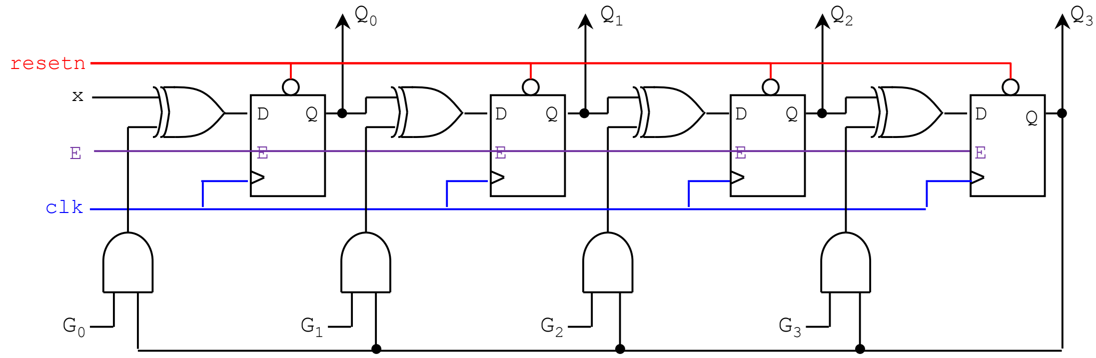
Solutions - Homework 4

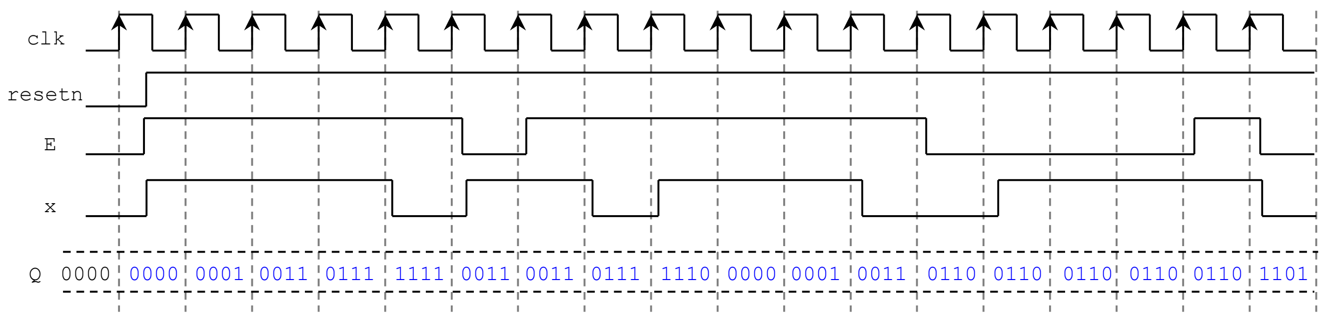
(Due date: November 17th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (15 PTS)

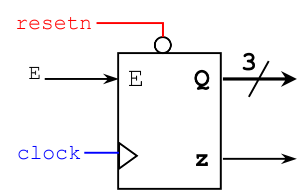
- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1101$, $Q = Q_3Q_2Q_1Q_0$





PROBLEM 2 (20 PTS)

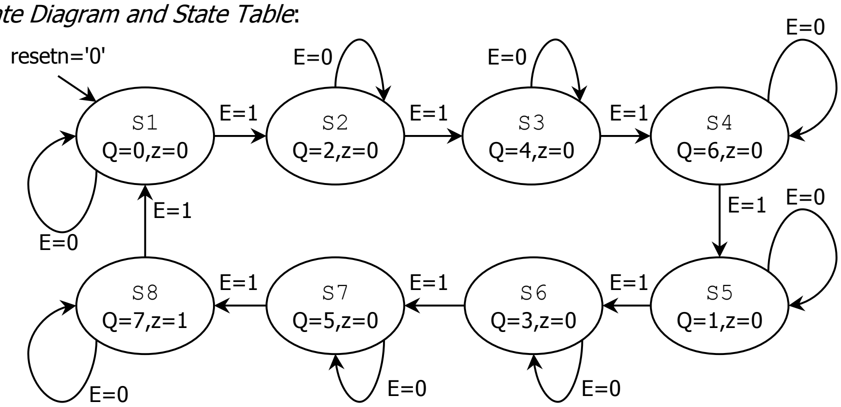
- Design a counter using a Finite State Machine (FSM):
  Counter features:
  ✓ Count: **000**, 010, 100, 110, 001, 011, 101, 111, **000**, 010, 100, ...
  ✓ $resetn$: Asynchronous active-low input signal. It initializes the count to '000' .
  ✓ Input E: Synchronous input that increases the count when it is set to '1'.
  ✓ output z: It becomes '1' when the count is 111.



Counter

- Provide the State Diagram (any representation), State Table, and the Excitation Table. Is this a Mealy or a Moore machine? Why? (10 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (5 pts)

- *State Diagram and State Table*:



E	PRESENT STATE	NEXT STATE	z
0	S1	S1	0
0	S2	S2	0
0	S3	S3	0
0	S4	S4	0
0	S5	S5	0
0	S6	S6	0
0	S7	S7	0
0	S8	S8	1
1	S1	S2	0
1	S2	S3	0
1	S3	S4	0
1	S4	S5	0
1	S5	S6	0
1	S6	S7	0
1	S7	S8	0
1	S8	S1	1

The output 'z' only depends on the present state ⇒ Moore FSM.

- *State Assignment and Excitation Table*:

  ✓ S1: Q = 000
  ✓ S2: Q = 010
  ✓ S3: Q = 100
  ✓ S4: Q = 110
  ✓ S5: Q = 001
  ✓ S6: Q = 011
  ✓ S7: Q = 101
  ✓ S8: Q = 111

PRESENT STATE				NEXTSTATE			
E	Q_2	Q_1	Q_0 (t)	Q_2	Q_1	Q_0 (t+1)	z
0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0
0	1	0	0	1	0	0	0
0	1	1	0	1	1	0	0
0	0	0	1	0	0	1	0
0	0	1	1	0	1	1	0
0	1	0	1	1	0	1	0
0	1	1	1	1	1	1	1
1	0	0	0	0	1	0	0
1	0	1	0	1	0	0	0
1	1	0	0	1	1	0	0
1	1	1	0	0	0	1	0
1	0	0	1	0	1	1	0
1	0	1	1	1	0	1	0
1	1	0	1	1	1	1	0
1	1	1	1	0	0	0	1

- *Excitation equations and minimization:*

$$Q_2(t+1) = \bar{E}Q_2 + Q_2\overline{Q_1} + E\overline{Q_2}Q_1 = \overline{EQ_1}Q_2 + EQ_1\overline{Q_2}$$
$$= Q_2 \oplus (EQ_1)$$
$$Q_1(t+1) = \bar{E}Q_1 + E\overline{Q_1}$$
$$Q_0(t+1) = \overline{Q_1}Q_0 + \bar{E}Q_0 + \overline{Q_2}Q_0 + EQ_2Q_1\overline{Q_0}$$
$$= \overline{EQ_2Q_1}Q_0 + EQ_2Q_1\overline{Q_0} = Q_0 \oplus (EQ_2Q_1)$$
$$z = Q_2Q_1Q_0$$

Q_2(t+1)

Q_1Q_0 \ EQ_2	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	1	0	1
10	0	1	0	1

Q_1(t+1)

Q_1Q_0 \ EQ_2	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	1	1	0	0
10	1	1	0	0

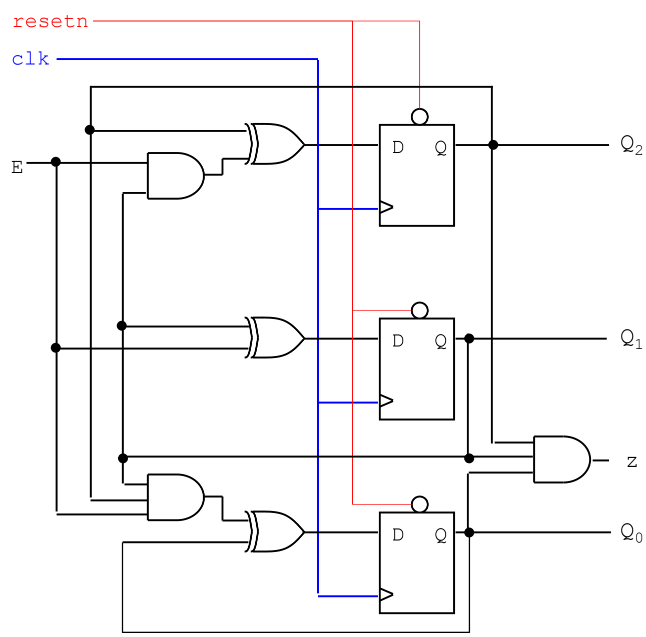
Q_0(t+1)

Q_1Q_0 \ EQ_2	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	0	1
10	0	0	1	0

z

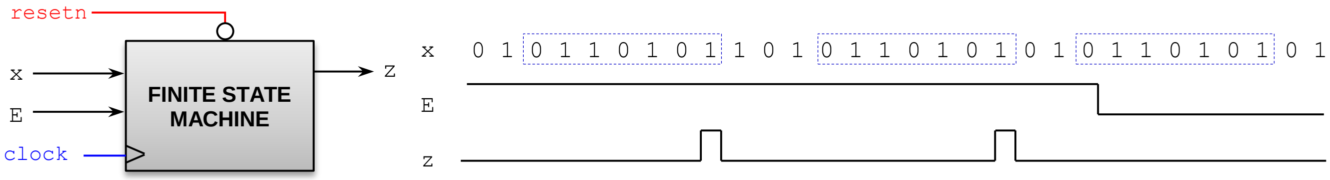
Q_1Q_0 \ EQ_2	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	1	1	0
10	0	0	0	0

- *Circuit Implementation:*

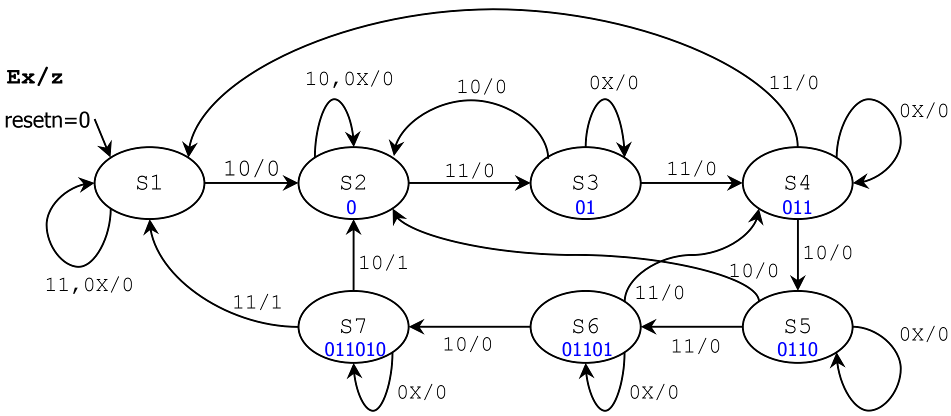


PROBLEM 3 (30 PTS)

- Sequence detector: Provide the State Diagram (any representation) and the Excitation Table of a circuit with an input x and output z. The machine has to generate $z = 1$ when it detects the sequence 0110101. Right after the sequence is detected, the circuit looks for a new sequence. (10 pts).
  The signal E is an input enable: It validates the input x, i.e., if $E = 1$, x is valid, otherwise x is not valid. The figure below illustrates the behavior for a certain input stream.



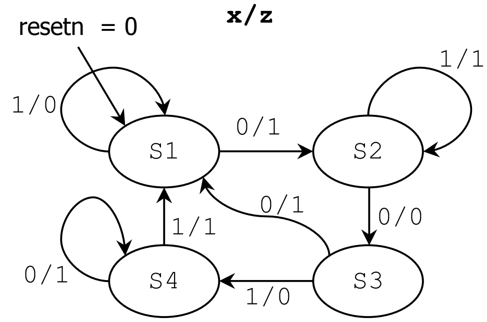
S1: Q=000
S2: Q=001
S3: Q=010
S4: Q=011
S5: Q=100
S6: Q=101
S7: Q=110

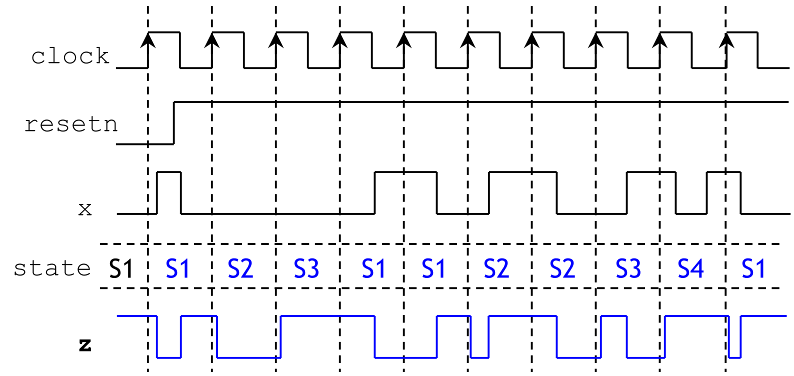


E	x	PRESENT STATE	NEXT STATE	z
0	X	S1	S1	0
0	X	S2	S2	0
0	X	S3	S3	0
0	X	S4	S4	0
0	X	S5	S5	0
0	X	S6	S6	0
0	X	S7	S7	0
1	0	S1	S2	0
1	0	S2	S2	0
1	0	S3	S2	0
1	0	S4	S5	0
1	0	S5	S2	0
1	0	S6	S7	0
1	0	S7	S2	0
1	1	S1	S1	0
1	1	S2	S3	0
1	1	S3	S4	0
1	1	S4	S1	0
1	1	S5	S6	0
1	1	S6	S4	0
1	1	S7	S1	1

		PRESENT STATE			NEXTSTATE			
E	x	$Q_2Q_1Q_0(t)$			$Q_2Q_1Q_0(t+1)$			z
0	X	0	0	0	0	0	0	0
0	X	0	0	1	0	0	1	0
0	X	0	1	0	0	1	0	0
0	X	0	1	1	0	1	1	0
0	X	1	0	0	1	0	0	0
0	X	1	0	1	1	0	1	0
0	X	1	1	0	1	1	0	0
1	0	0	0	0	0	0	1	0
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	1	0
1	0	0	1	1	1	0	0	0
1	0	1	0	0	0	0	1	0
1	0	1	0	1	1	1	0	0
1	0	1	1	0	0	0	1	0
0	1	0	0	0	0	0	0	0
0	1	0	0	1	0	1	0	0
0	1	0	1	0	0	1	1	0
0	1	0	1	1	0	0	0	0
0	1	1	0	0	1	0	1	0
0	1	1	0	1	0	1	1	0
0	1	1	1	0	0	0	0	1
X	X	1	1	1	X	X	X	X

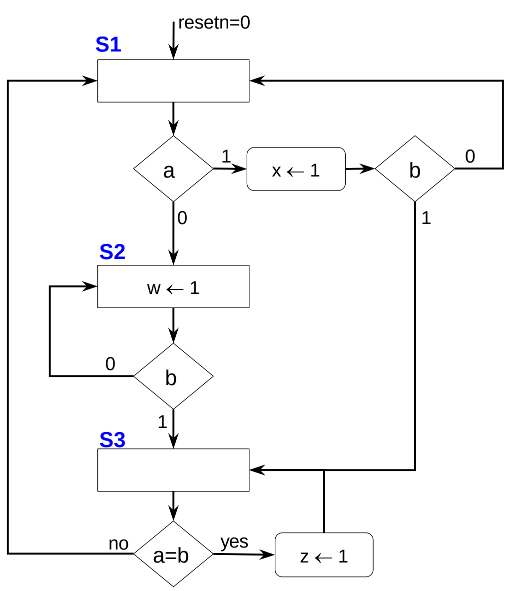
- Complete the timing diagram of the following FSM. Is this a Mealy or a Moore machine? Why? (5 pts)



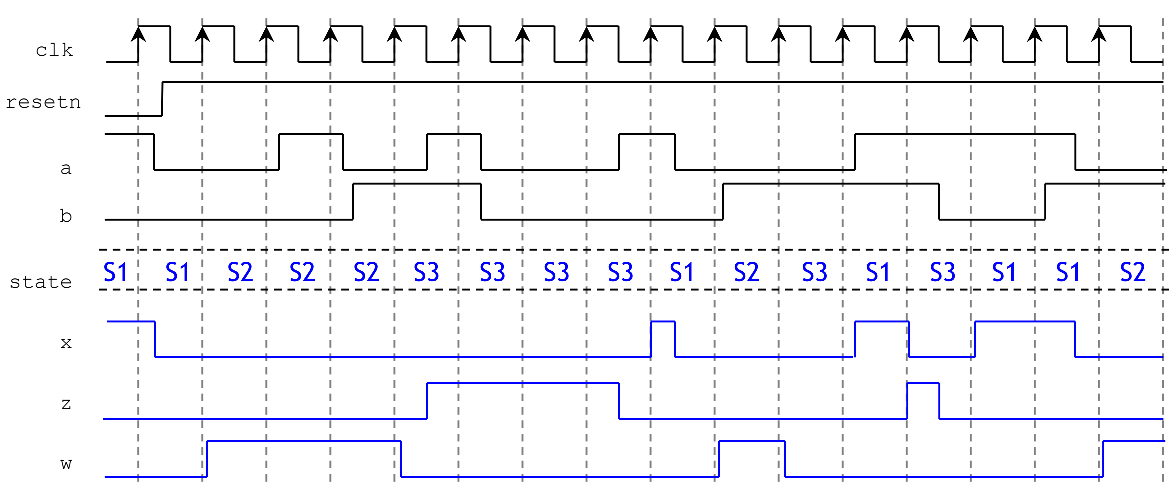


- Provide the state diagram (in ASM form) and complete the timing diagram of the FSM whose VHDL description is listed below. (15 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, resetn: in std_logic;
          a, b: in std_logic;
          x,w,z: out std_logic);
end circ;
```

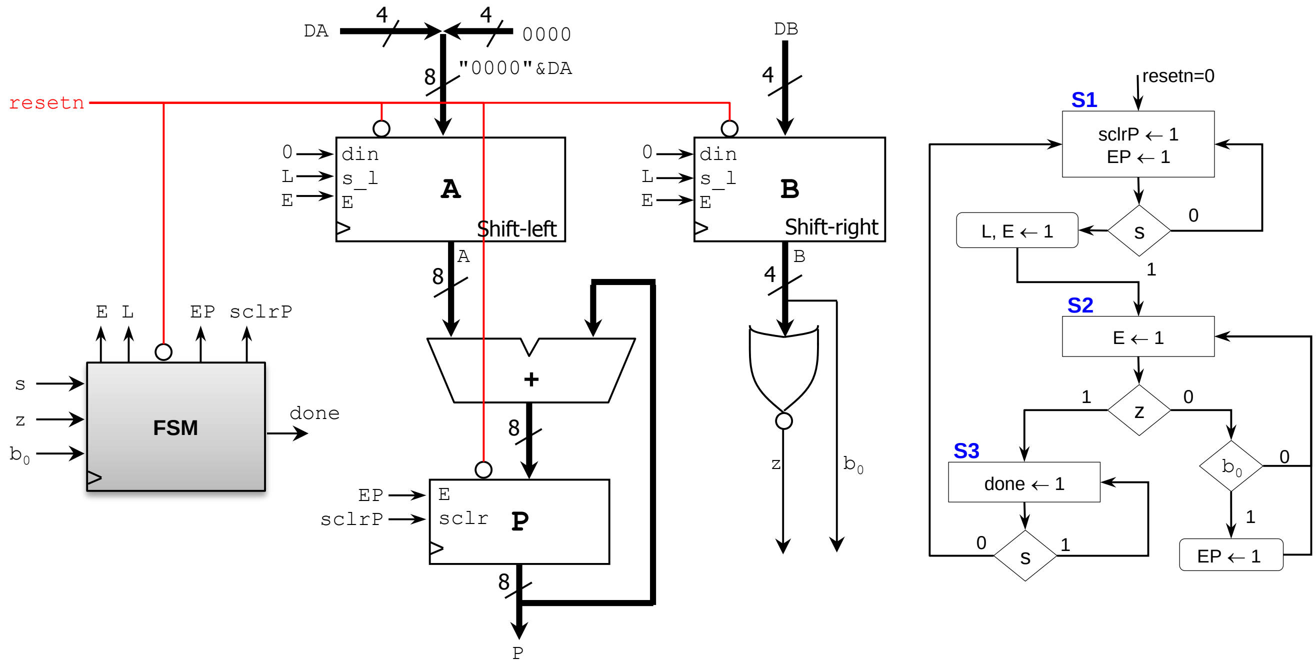


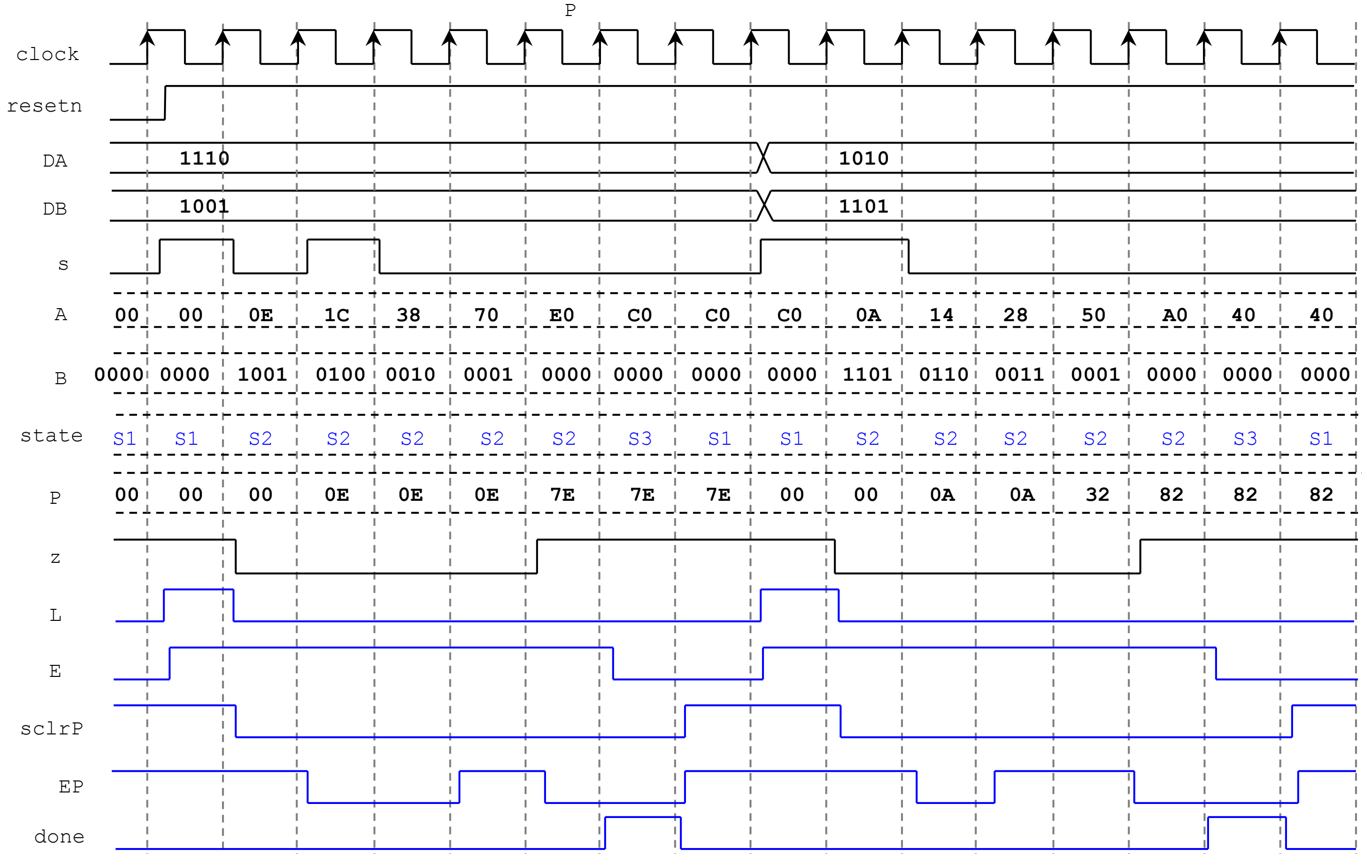

```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, a, b)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if a = '1' then
              if b = '1' then y <= S3; else y <= S1; end if;
            else
              y <= S2;
            end if;

          when S2 =>
            if b = '1' then y <= S3; else y <= S2; end if;

          when S3 =>
            if a = b then y <= S3; else y <= S1; end if;
        end case;
     end if;
  end process;

  Outputs: process (y, a, b)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if a = '1' then x <= '1'; end if;
         when S2 => w <= '1';
         when S3 => if a = b then z <= '1'; end if;
      end case;
  end process;
end behavioral;
```



PROBLEM 4 (20 PTS)

- Complete the following timing diagram (`A` and `P` are specified as hexadecimals) of the following Iterative unsigned multiplier. The circuit includes an FSM (in ASM form) and a datapath circuit.
  Register (for `P`): $sclr$: synchronous clear. Here, if $sclr = E = 1$, the register contents are initialized to 0.
  Parallel access shift registers (for `A` and `B`): If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift





PROBLEM 5 (15 PTS)

- Attach a printout of your Project Status Report (no more than two pages, single-spaced, 2 columns). This report should contain the current status of the project. You **MUST** use the provided template (`Final Project – Report Template.docx`).